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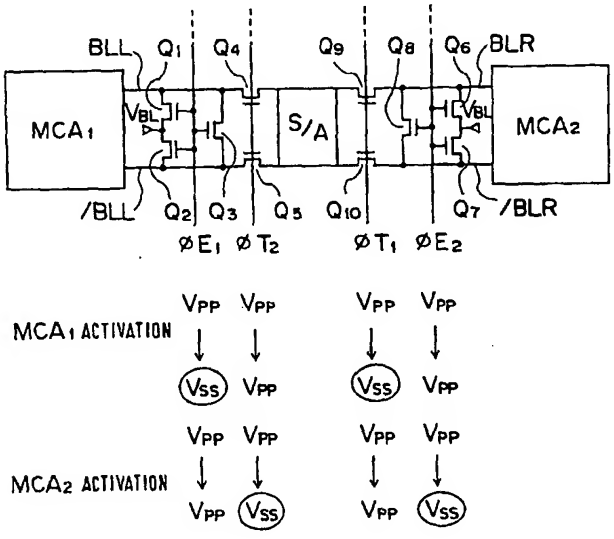
(54) Semiconductor memory device

(57) A semiconductor device is constituted by a booster circuit, memory cell arrays (MCA1, MCA2), a sense amplifier circuit (S/A), transmission gate circuits (Q4, Q5; Q9, Q10), equalizing circuits (Q1, Q2, Q3; Q6, Q7, Q8) and a control circuit applying a boosted potential respectively to the gates of MOS transistors of the transmission gate circuits and the equalizing circuits when no memory cells of the memory cell arrays are selected whereby the capacitance of de-coupling capacitors connected to output terminals of the booster circuit can be reduced thereby contributing to reduction in chip area.

Fig.1



EP 0 717 415 A2

Fig. 1 is a circuit diagram of the semiconductor memory of the present invention showing essential parts, and an operation diagram thereof;

Fig. 2 is a circuit diagram of the semiconductor memory, showing more details of the essential part in Figure 1 and the control circuit thereof;

Fig. 3. is an entire circuit configuration diagram of the embodiment of the present invention;

Fig. 4 is a plane view of the semiconductor memory device of the embodiments of the present invention, showing details of the essential parts of Fig.3;

Fig. 5 is a structural diagram of a booster circuit of a semiconductor memory device of the embodiments ;

Fig. 6 is a view showing operational characteristic of the booster circuit of Fig. 5;

Fig. 7 is a circuit diagram showing in details the booster circuit of Fig. 5;

Fig. 8 is a circuit diagram showing in details the booster circuit of Fig. 5 ;

Fig. 9 is a circuit diagram showing in details the booster circuit of Fig. 5;

Fig. 10 is an operation diagram of the circuits shown in Figs. 7, 8 and 9;

Fig. 11 is a plane view showing locations of decoupling capacitors; and

Fig. 12 is a circuit diagram showing in details a word line driving circuit and a row decode circuit.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Embodiments of the present invention will be described in detail with reference to the drawings.

Although the present invention is naturally applicable to various semiconductor memory devices (SRAM, EPROM, MROM etc.) the explanation will be given of a DRAM since the present invention is preferable to a DRAM.

Fig. 1 shows essential parts of the present invention which are constituted by a first memory cell array MCA1, a second memory cell array MCA2, a pair of left bit lines BLL and /BLL, a pair of right bit lines BLR and /BLR, a sense amplifier S/A and the like. Further, the embodiment includes a left bit line pair equalizing circuit constituted by N-channel MOS transistors Q1, Q2 and Q3, a left transmission gate constituted by N-channel MOS transistors Q4 and Q5, a right bit line pair equalizing circuit constituted by N-channel MOS transistors Q6, Q7 and Q8 and a right transmission gate circuit constituted by N-channel MOS transistors Q9 and Q10. A plurality of dynamic type memory cells are arranged in a matrix in each of the memory cell arrays MCA1 and MCA2. The memory cells belonging to the same column are connected by the same pair of bit lines and the memory cells belonging to the same row are connected by the same word line. The left bit line pair equalizing circuit is controlled by a signal ϕ E1. When ϕ E1 is at a boosted potential Vpp (for example, 4.3V in comparison with ground potential), VBL (for example, 1.5V which is about a half of potential of VDD that is an inner power source potential) is supplied to the left bit line pair BLL and /BLL and the both are shortcircuited. When ϕ E1 is at a ground potential Vss (0V) all the MOS transistors in the circuit are made nonconductive. The right bit line pair equalizing circuit is controlled by a signal ϕ E2. When ϕ E2 is at the boosted potential Vpp, VBL is supplied to the right bit line pair BLR and /BLR and the both are shortcircuited. When ϕ E2 is at the ground potential Vss, all the MOS transistors in the circuit are made nonconductive. The left transmission gate circuit is controlled by a signal ϕ T2. When ϕ T2 is at the boosted potential Vpp, the left bit line pair BLL and/BLL is connected to the sense amplifier S/A . When ϕ T2 is at the ground potential Vss, the left bit line pair BLL and /BLL and the sense amplifier S/A are disconnected from each other. The right transmission gate circuit is controlled by a signal ϕ T1. When ϕ T1 is at the boosted potential Vpp, the right bit line pair BLR and /BLR are connected to the sense amplifier S/A. When ϕ T1 is at the ground potential Vss, the right bit line pair BLR and/BLR and the sense amplifier S/A are disconnected from each other.

In the above-constituted DRAM when none of the memory cells in the first and the second memory cell arrays is selected, all of ϕ E1, ϕ E2, ϕ T1, ϕ T2 are connected to Vpp. Since a word line, not shown, is in a nonselect state, data stored in the memory cells are not destructed. At this moment all the MOS transistors Q1 through Q10 in Fig. 1 are connected to Vpp and accordingly, the transistors provide a parasitic capacitance connected in parallel to capacitive elements that are to be connected to output terminals of a booster circuit, not shown, by which the capacitive elements can be made smaller by the amount of the parasitic capacitance.

When the memory cells in the first memory cell array are selected, as shown in Fig. 1, ϕ E1 is changed from Vpp to Vss, ϕ T2 is maintained as Vpp, ϕ T1 is changed from Vpp to Vss and ϕ E2 is maintained as Vpp by which the sense amplifier S/A and the second memory cell array MCA2 are disconnected from each other and the equalizing operation of the left equalizing circuit is released.

When the memory cells in the second memory cell array are selected, in a similar way, ϕ E1 is maintained as Vpp, ϕ T2 is changed from Vpp to Vss, ϕ T1 is maintained as Vpp and ϕ T2 is changed from Vpp to Vss by which the sense amplifier S/A and the first memory cell array MCA1 are disconnected from each other and the equalizing operation of the right equalizing circuit is released.

As stated above by using the transistors of the transmission gates and the like which have conventionally been connected to the ground potential in a nonselect time as a capacitor of the booster circuit, the area of the capacitive elements can be reduced by the amount of their parasitic capacitance.

Next, Fig. 2 shows essential parts of the present invention and the details of a control system. The control

BNSDOCID <EP_ 0717415A2 I >

select line is used for partial activation of the sense amplifier circuits and for driving the column gate circuits. The memory cell block constitutes the 16M bits core block CB by dividing it into top and bottom groups between which respectively arranged are row decoder circuits R/D(23) each corresponding to each memory cell array, circuits WDRV for supplying drive signals to the row decoder circuits, circuits RFUSE for holding replaced data of row redundancy circuits, data line amplifying circuits DQB, a block control circuit BC and the like. P-channel type sense amplifier drive circuits PSAD each corresponding to each peripheral circuit within a core section are respectively arranged at peripheral portions of the core blocks CB.

The memory cell arrays MCA1 and MCA2 shown in Fig. 1 and Fig. 2 respectively correspond to the memory cell arrays Cell in Fig. 4. As is illustrated one 16M core block CB has 64 of the memory cell arrays Cell (MCA) and a single chip has 256 of the memory cell arrays Cell (MCA). The following description indicates how much parasitic capacitance is provided by the block structure shown in Fig. 3 and Fig. 4 and how much capacity of the de-coupling capacitor can be saved as a result.

First, a contribution of the transmission gate circuits will be calculated. There are 1024 pairs of bit lines in one memory cell array (disregarding redundancy bit lines). Therefore, the number of the transmission gate circuits in a single chip is 262144. Incidently, a single transmission gate circuit is constituted by two N-channel transistors. Therefore, the number of the MOS transistors in the transmission gate circuits is 524288. For example, assuming the gate width of 0.8mm and the gate length of 0.56μm in one MOS transistor, the area of the channel regions in one MOS transistor is 0.45μm^2. By multiplying the area to all the MOS transistors the area amounts to 234880μm^2. Assuming the gate oxide film thickness of 12nm, it corresponds to a parasitic capacitance of 0.68nF.

Secondly, a contribution of the equalizing circuits will be calculated. The number of the equalizing circuits in a single memory cell array is also 262144. A single equalizing circuit is constituted by three MOS transistors, that is, two MOS transistors each having the gate width of 0.8μm and the gate length of 0.56μm and one MOS transistor having the gate width of 2.0μm and the gate length of 0.56μm. Accordingly, when the area is multiplied to all the MOS transistors, the total area of the channel regions amounts to 528482μm^2. This corresponds to a parasitic capacitance of 1.52nF.

The parasitic capacitance calculated as above amounts to approximately 2.2nF. Normally several (4 in a refresh cycle product having 8K and 8 in a refresh cycle product having 4K) memory cell arrays are selected in reading. Therefore, substantially all of the memory cell arrays contribute to the parasitic capacitance. Further, in a 64M DRAM, a de-coupling capacitor DC having a capacitance of approximately 5nF is necessary to guarantee a stable operation. However, it is possible to approximately halve it to 2.8nF by the circuit structure of the present invention which contributes to a considerable reduction in the chip area.

In this way, the memory device is divided into a number of memory cell arrays as in a DRAM having a large capacity and a ratio of the number of the memory cell arrays that are simultaneously activated to a total thereof is reduced by which the total amount of the parasitic capacitance can be increased which as a result contributes to the considerable reduction in the chip area.

Further, as shown in Fig. 11 the de-coupling capacitors DC are scattered all over the tip.

Next, a detailed explanation will be given of the booster circuit VPPGEN in reference to Fig. 5 through Fig. 10.

Fig. 5 shows the circuit structure of the booster circuit VPPGEN. The booster circuit is constituted by a reference potential generating circuit 50, comparing circuits 51,52 and 53, ring oscillator circuits 54,55 and 56, driver circuits 57,58 and 59, charge pump circuits 60,61 and 62, voltage dividing circuits 63,64 and 65 and a power source voltage step-down transistor Q66. As shown in Fig. 5, an outer potential Vcc inputted from the outside is stepped down by the power source voltage step-down transistor Q66 whereby VDD is generated and VDD is again boosted by the charge pump circuits 60 and 61 whereby the boosted potential Vpp is generated. The power source voltage step-down transistor Q66 is driven by VPPD that is a potential boosted from VDD. Further, the generation of Vpp is performed by two kinds of systems, that is, a system exclusive for standby and a system exclusive for operation. In this way the booster circuit is constituted by three booster systems each performing the boosting operation independently by a feedback type control.

Fig. 6 shows behaviors of changes of Vpp, VPPD and VDD with respect to Vcc along with those of a cell capacitor plate potential VPL, a bit line potential VBL and a substrate potential VBB. There is a nonvariational region of potentials between approximately 3V to approximately 4V.

Fig. 7 shows the detail of the ring oscillator 54 and a portion of the driver circuit 57. In the ring oscillator 54 a NAND gate 541 and even number stages of inverters 542, 543, 544, 545, 546 and 547 are connected in a ring-like form. In the driver circuit inverter circuits 571,572, 573, 574, 575, 576, 578, 579, 580, 581, 582, 583 and 584 are connected in series respectively forming successively delayed signal outputs /C0, C0, /C1, C1, /C2, C2, /C3, C3, /C4, C4, /C5, C5, /C6 and C6.

Fig. 8 shows the remaining portion of the driver circuit 57. A signal A1 is formed from the signals C1 and C4 by a NAND gate 585 and inverters 586, 587 and 589. A signal B1 is formed from the signals C1 and C6 by a NAND gate 590 and inverters 591, 592 and 593. A signal C11 is formed from the signals C3, /C6,C2 and /C0 by a ANDNOR gate 604 and inverters 605, 606 and 607. A signal C12 is formed from the signals C3,/C6,C2 and/C0 by an ORNAND gate 608 and inverters 609,610,611 and

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in the first equalizing circuit and the gates of the transistors in the second transmission gate circuit and applies the boosted potential respectively to the gates of the transistors in the second equalizing circuit and the gates of the transistors in the first transmission gate circuit when selecting the memory cells in the first memory cell array; and

wherein the control circuit applies the ground potential respectively to the gates of the transistors in the second equalizing circuit and the gates of the transistors in the first transmission gate circuit and applies the boosted potential respectively to the gates of the transistors in the first equalizing circuit and the gates of the transistors in the second transmit circuit when selecting the memory cells in the second memory cell array.

3. A semiconductor memory device comprising:

a booster circuit for generating a boosted potential;

a first memory cell array including first pairs of bit lines;

a second memory cell array including second pairs of bit lines;

a sense amplifier circuit;

a first transmission gate circuit having pairs of transistors for connecting the first pairs of bit lines to the sense amplifier circuit;

a second transmission gate circuit having pairs of transistors for connecting the second paris of bit lines to the sense amplifier circuit; and

a control circuit applying the boosted potential respectively to gates of the transistors in the first and the second transmission gate circuits when none of memory cells in the first and the second memory cell arrays is selected.

4. The semiconductor memory device according to Claim 3, wherein the control circuit applies a ground potential to the gates of the transistors in the second transmission gate circuits and applies the boosted potential to the gates of the transistors in the first transmission gate circuit when selecting the memory cells in the first memory cell array; and

the control circuit applies the ground potential to the gates of the transistors in the first transmission gate circuit and applies the boosted potential to the gates of the transistors in the second transmission gate circuit when selecting tee memory cells in the second memory cell array.

5. The semiconductor memory device according to Claim 2 or 4, wherein first and second word line driving circuits are respectively connected to the first and the second memory cell arrays and the first and the second word line driving circuits are operated by the boosted potential.

6. The semiconductor memory device according to Claim 5, wherein the first and the second word line driving circuits are controlled respectively based on selection signals of first and second row decode circuits and the first and the second row decode circuits are operated by the boosted potential.

7. The semiconductor memory device according to Claim 1 or 6, wherein the control circuit comprises at least a first level shift circuit for shifting an amplitude level of a first select signal for selecting the first memory cell array to a level of the boosted potential and a second level shift circuit for shifting an amplitude level of a second select signal for selecting the second memory cell array to the level of the boosted potential and the boosted potential is used for a power source of the first and the second level shift circuits.

8. The semiconductor memory device according to Claim 7, wherein the control circuit is further comprising first and second drive circuits respectively connected to the first and the second level shift circuits, said first and second drive circuits using the boosted potential as a power source and driving the gates of the transistors in the first and the second transmission gate circuits to the boosted potential when none of the memory cells in the first and the second memory cell arrays is selected.

9. The semiconductor memory device according to Claim 1 or 3, wherein capacitive elements are connected to the output of the booster circuit.

10. The semiconductor memory device according to claim 1 or 3, wherein the booster circuit generates the boosted potential by stepping down a potential inputted from an outside and again boosting the potential.

11. The semiconductor memory device according to Claim 7, wherein the control circuit is further comprising first and second drive circuits respectively connected to the first and the second level shift circuits, said first and second drive circuits using the boosted potential as a power source and driving the gates of transistors in the first and the second transmission gate circuits and the gates of transistors in the first and the second equalizing circuits to the boosted potential when none of the memory cells in the first and the second memory cell arrays is selected.

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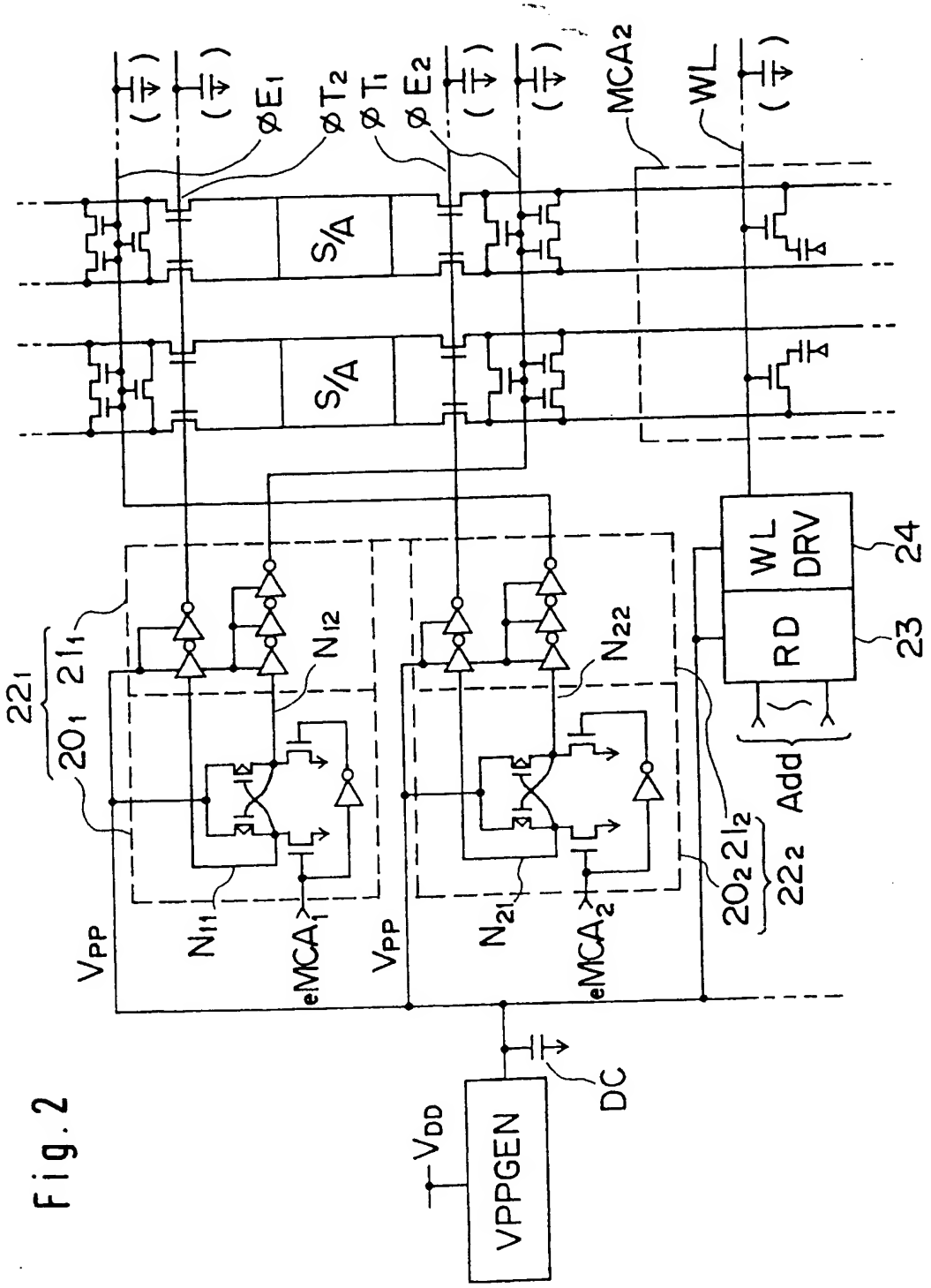

Fig. 2

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Fig.4

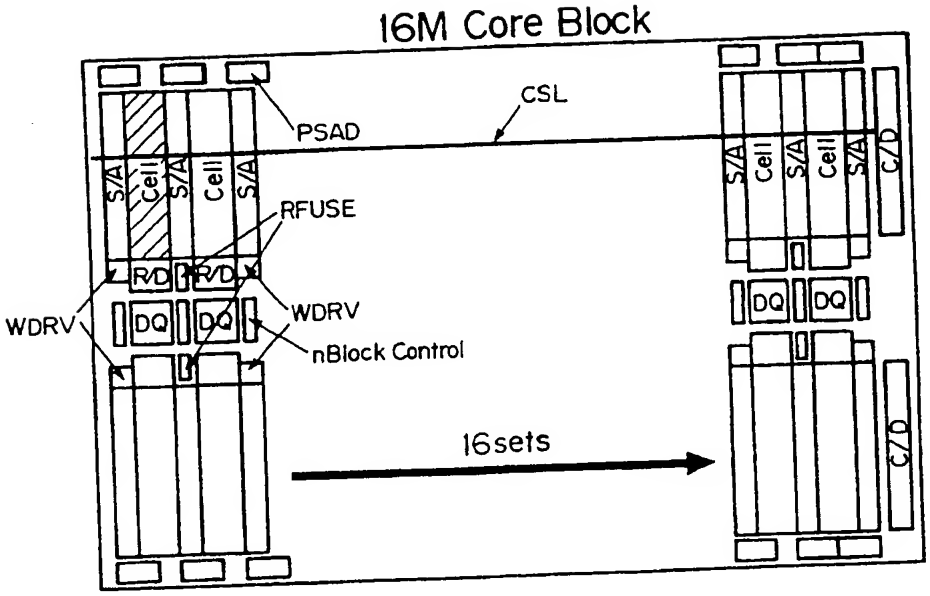

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Fig. 6

Output characteristic of internal voltage generator (normal 85°C)

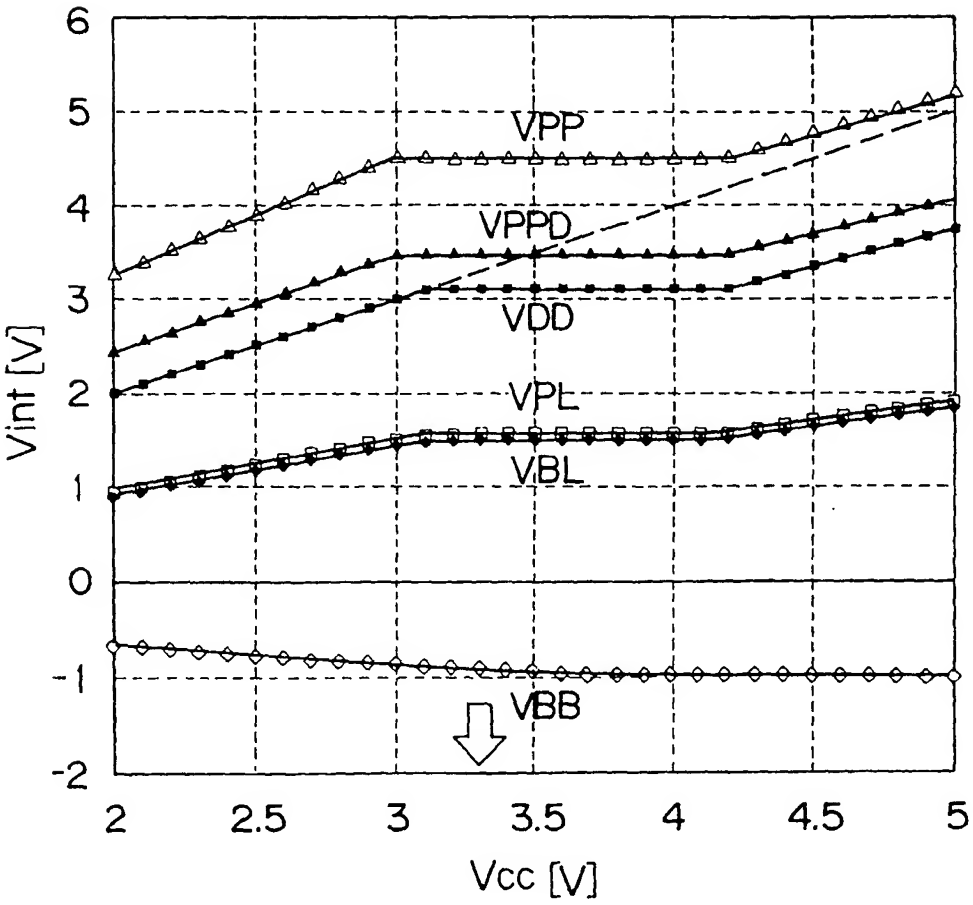

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Fig. 8

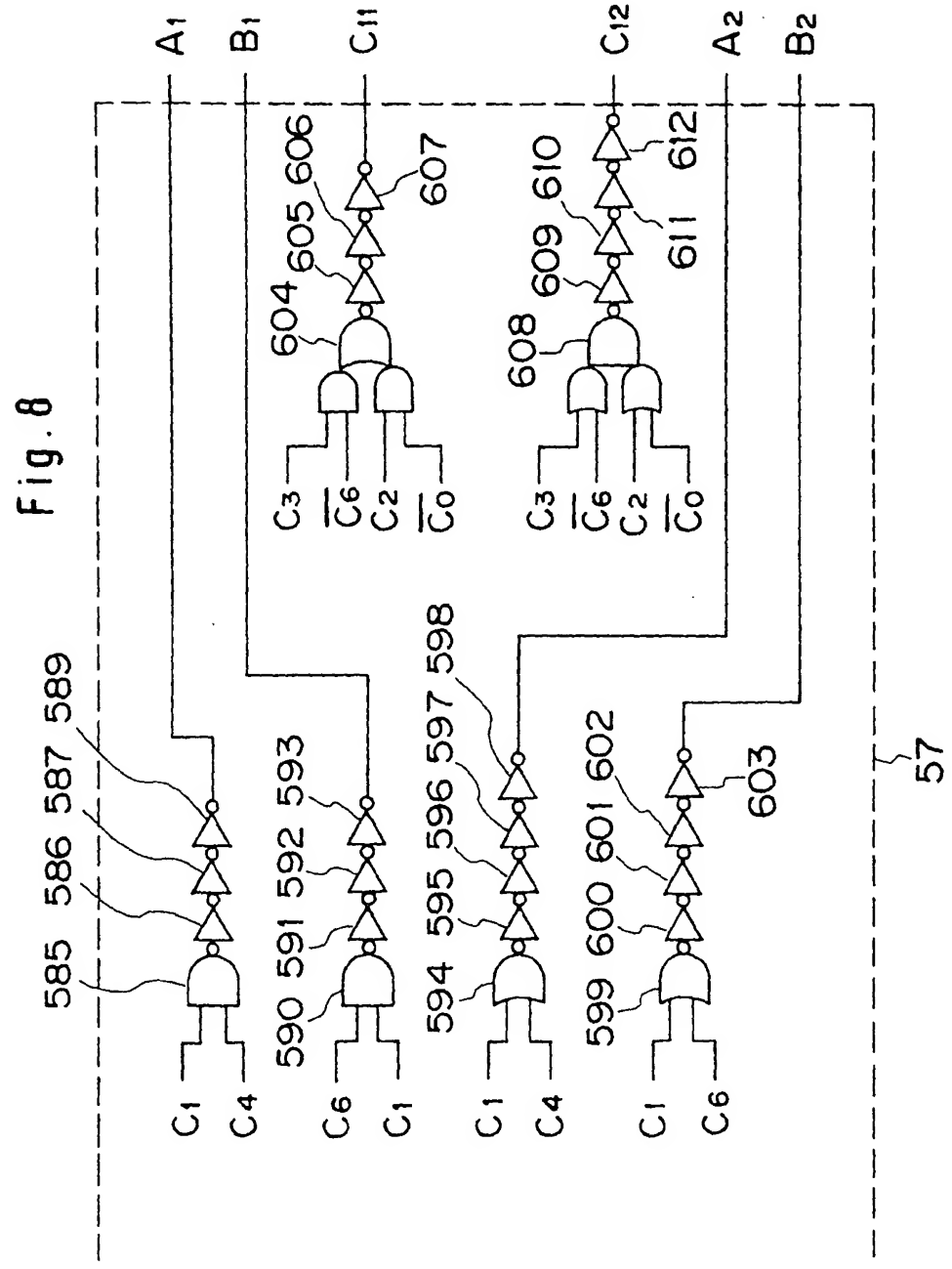

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Fig.10

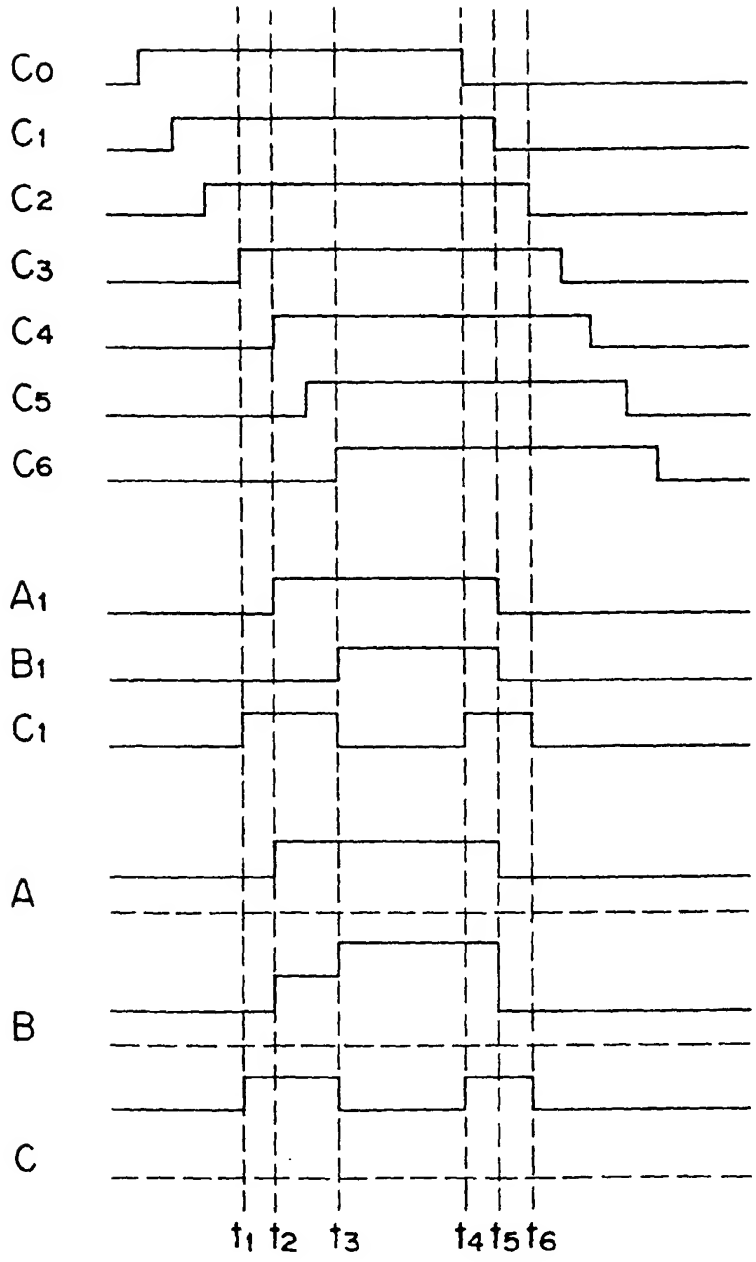

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Fig. 12

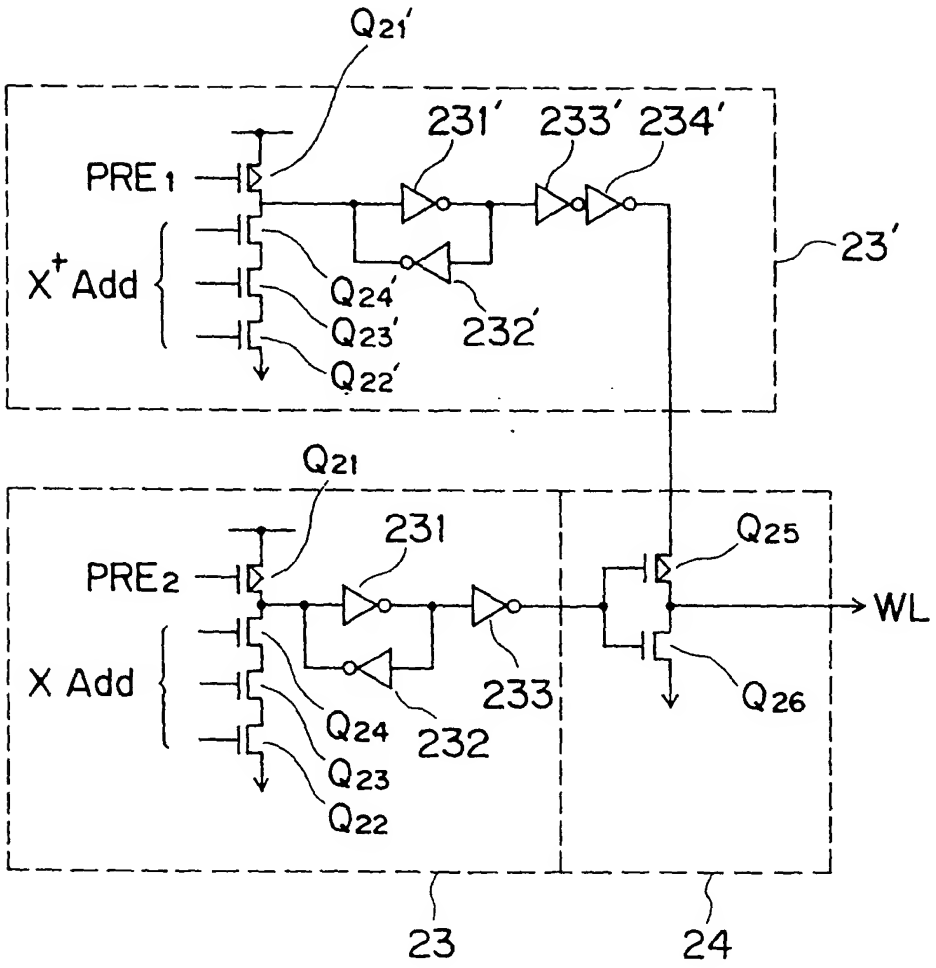

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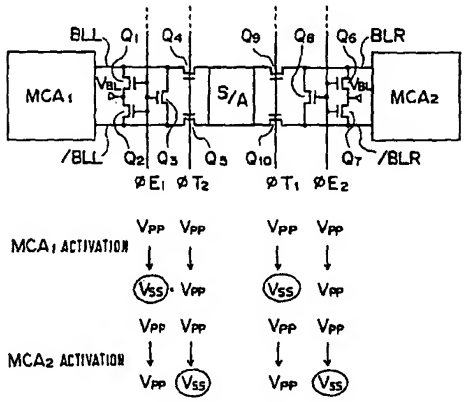
Fig.1



EP 0 717 415 A3

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